PATENT

IN THE UNITED STATES PATENT OFFICE

Applicants: Reno L. Sanchez et al.
Assignee: Xilinx, Inc.
Title: METHOD AND SYSTEM FOR INSERTING PROBE POINTS IN FPGA-BASED SYSTEM-ON-CHIP (SoC)
Serial No.: 10/082,517 File Date: 2-22-02
Examiner: Unassigned Art Unit: 2812
Docket No.: X-998 US

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the twelve (12) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D. C. 20231, on April 11, 2002.

Julie K. Adams — *Name*
Julie K Adams — *Signature*

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